Application Note 30

Using the RC6100 Horizontal Genlock Circuit in a Digital Video System

Description

The Raytheon RC6100 Horizontal Line Genlock integrated circuit accepts baseband composite video, composite sync, or separate horizontal and vertical sync signals; provides support for both NTSC and PAL signal formats; provides a choice of eight pixel-clock frequencies; and provides the following control signals that are useful for digital video processing, composite sync, horizontal reset, horizontal frequency clock, clamp gate, vertical reset, field ID, and lock-detect indication. To provide stable output control signals, the RC6100 features a high-speed tracking sync separator that is tolerant of hum and average picture level (APL) fluctuations. The RC6100 includes a glitch-filter circuit for removal of impulse-noise. In addition, an input lowpass filter is provided for optional use in high-noise environments. It has a low-jitter PLL clock generator that can lock to and follow sync signals from VCRs. The RC6100 is designed to be simple to use, while still offering the video system designer the design flexibility they need.

Applications

The horizontal genlock function is used in several video processing applications including video conferencing, computer frame-grabber boards, studio broadcast equipment and video digitizing equipment. Figure 1 illustrates a typical application of the RC6100. The horizontal genlock IC locks to an incoming baseband composite video signal and generates a pixel clock and other control signals. The pixel clock and control signals are required for timing operations like video A/D conversion, digital signal processing, and video D/A conversion.

Figure 2 shows the circuitry required by the RC6100 for a typical NTSC application. Set NTSC/PAL = 1, S1 = 1 and S0 = 0, which corresponds to a sampling rate of four time the subcarrier frequency for NTSC systems.

Component Values

Table 1 provides standard values for programming the RC6100. Alternate programming values may be derived by using the following loop equations:

$KVCO = 2*\pi\ (fmx - fmn)/\Delta\ VIN$

- KVCO is the oscillator gain
- fmx is the maximum VCO output frequency
- fmn is the minimum VCO output frequency
- ΔVIN is the Phase Detector Range.

$Kcp = Ip/2\pi$

- Kcp is the phase detector and charge pump gain
- Ip is the charge pump current. In the example shown in Table 1, Ip = 240μA.

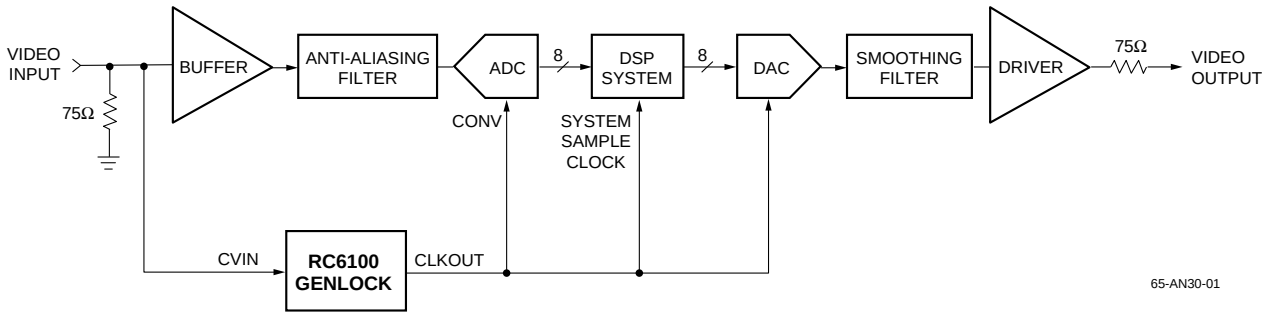


Figure 1. RC6100 Application in a Digital Video System

The PLL loop filter is approximated as an RC network from pin 24 to GND.

$R1 = (2\pi*n*m*fc)/KVCO*Kcp$

- n and m are divider coefficients
- fc is the 3dB point of the PLL loop. In the example shown in Table 1.

$fc = f_{IN}/20$

$C2 = 1/(2\pi*f2*R1)$

- $f2 = fc/10$

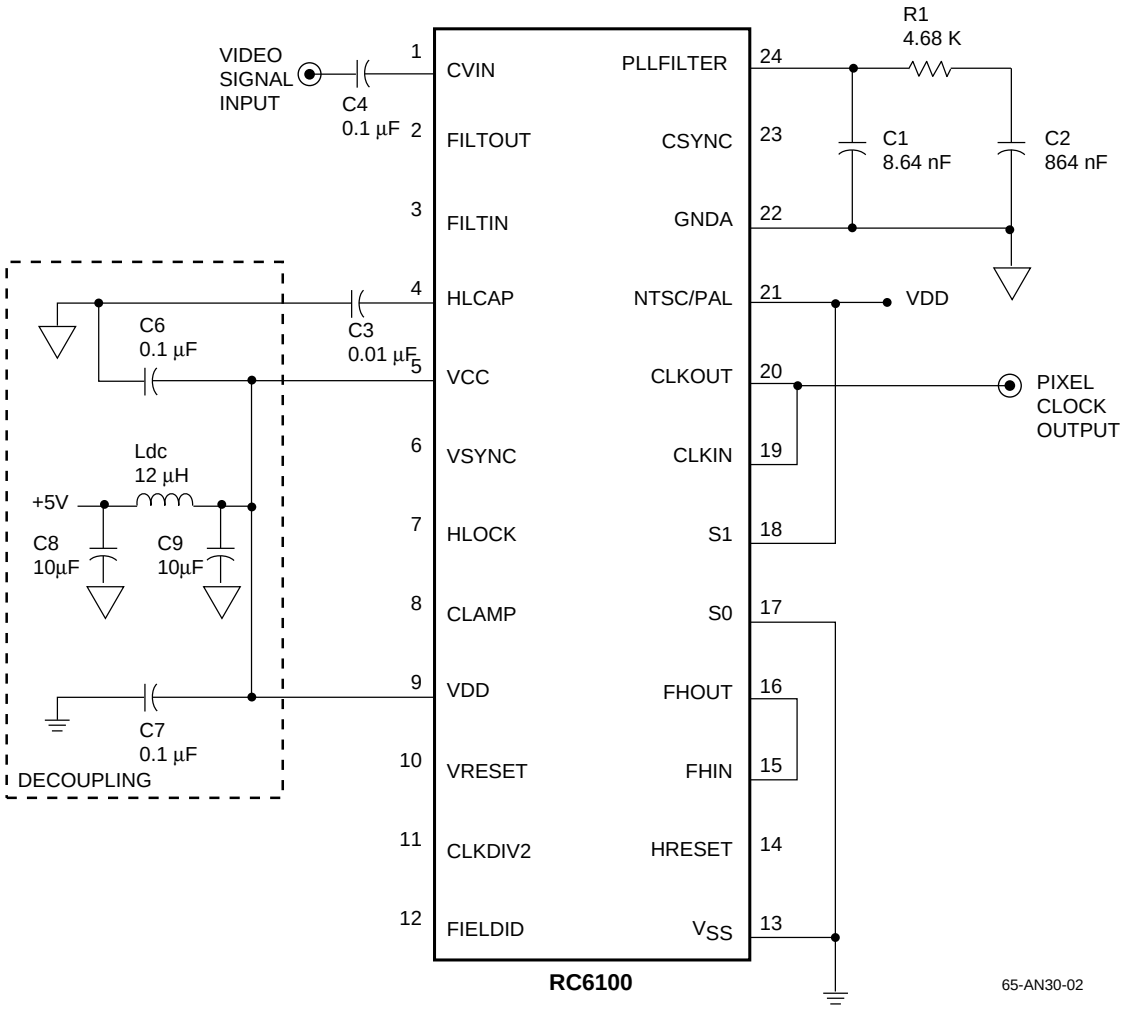
$C2/100<C1<C2/20$

Table 1. PLL Filter Component Vaules

Code	f_{IN}	fosc	div (n)	div (m)	KVCO	KCP	R1	C1	C2(K/20)
100	15734	27.00E+06	1.00	858	2.66E+07	3.82E-05	4.17E+03	9.69E-09	9.69E-07
101	15734	25.18E+06	1.00	800	2.66E+07	3.82E-05	3.89E+03	1.04E-08	1.04E-06
110	15734	14.32E+06	2.00	455	2.51E+07	3.82E-05	4.68E+03	8.64E-09	8.64E-07
111	15734	12.27E+06	2.00	390	2.51E+07	3.82E-05	4.01E+03	1.01E-08	1.01E-06
000	15625	27.00E+06	1.00	864	2.66E+07	3.82E-05	4.17E+03	9.76E-09	9.76E-07
001	15625	17.73E+06	2.00	567.5	3.48E+07	3.82E-05	4.19E+03	9.72E-09	9.72E-07
010	15625	15.00E+06	2.00	480	2.48E+07	3.82E-05	4.97E+03	8.19E-09	8.19E-07
011	15625	14.75E+06	2.00	472	2.48E+07	3.82E-05	4.89E+03	8.33E-09	8.33E-07

Notes:

1. Code: = <NTSC/PAL> <S1> <S0>
2. Constants are based on simulation results, actual values may differ.
3. Table values are ideal; actual values may be ±20% due to process variations.



Notes:

1. Decouple VCC, VDD inputs to ground with a 0.1 µF chip capacitor.
2. Use a separate trace to each power plane pin and place capacitors next to part.
3. Use separate ground plane for digital signals and PLL signals.

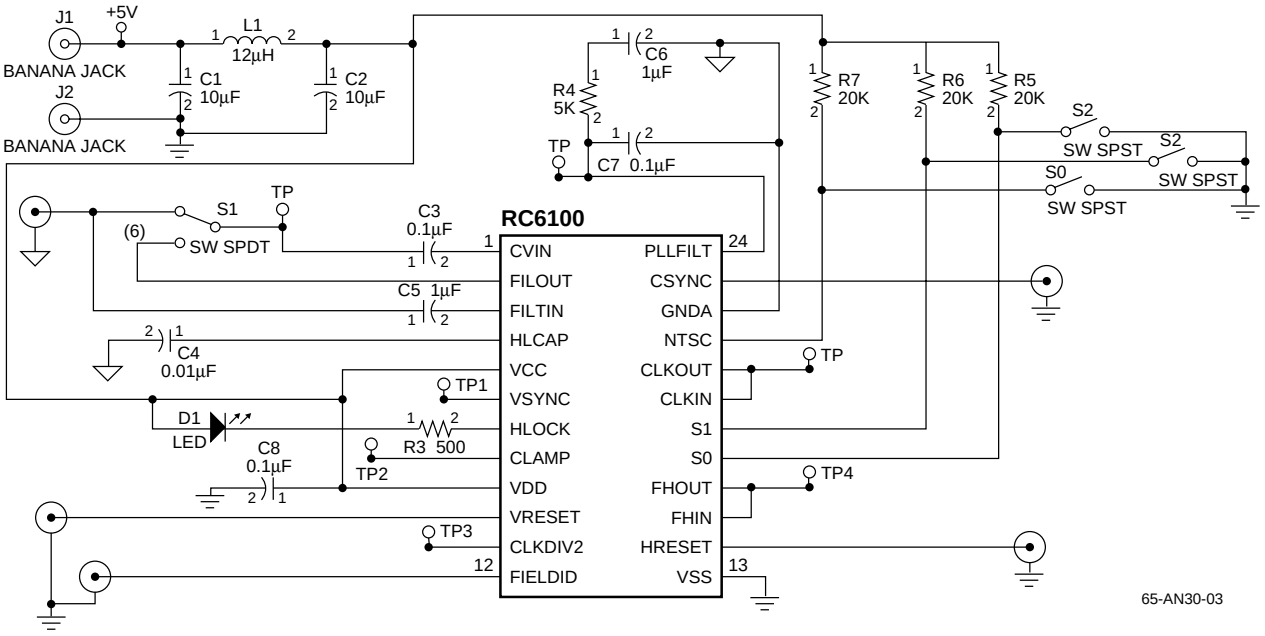
▽ PLL

⏚ Digital

4. Place PLL filter components as close as possible to pin 24.

Figure 2. RC6100 Application Diagram for NTSC Signals

Test Card



Notes:

1. NTSC/PAL switches; ON means switch is grounded. For example, PAL 27MHz CODE 000 all switches on, left position when looking at board.
2. The switch near the video input connects that BNC to pin 1 in the direct position and to pin 3 in the filter position.

Figure 3. RC6100 Prototype Test Card

Waveforms

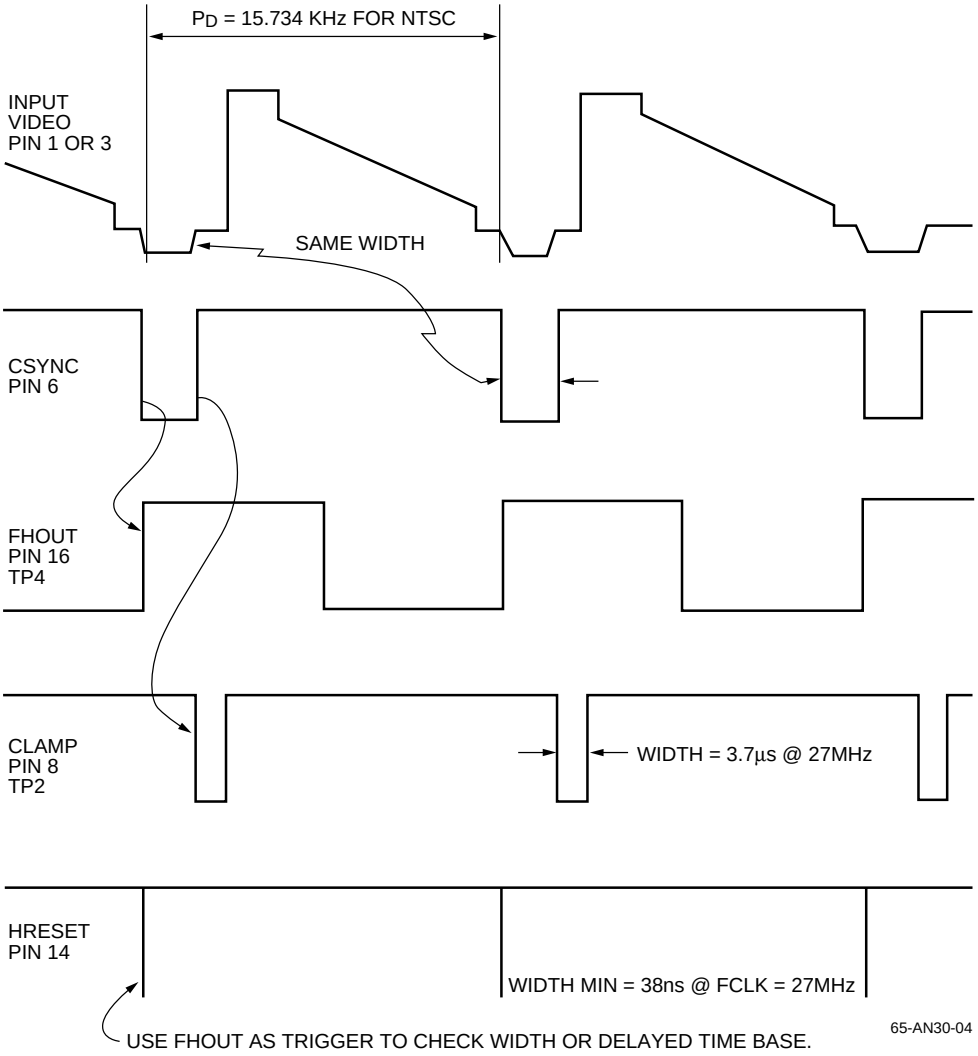


Figure 4. Device and Demo Board Waveform

Waveforms (continued)

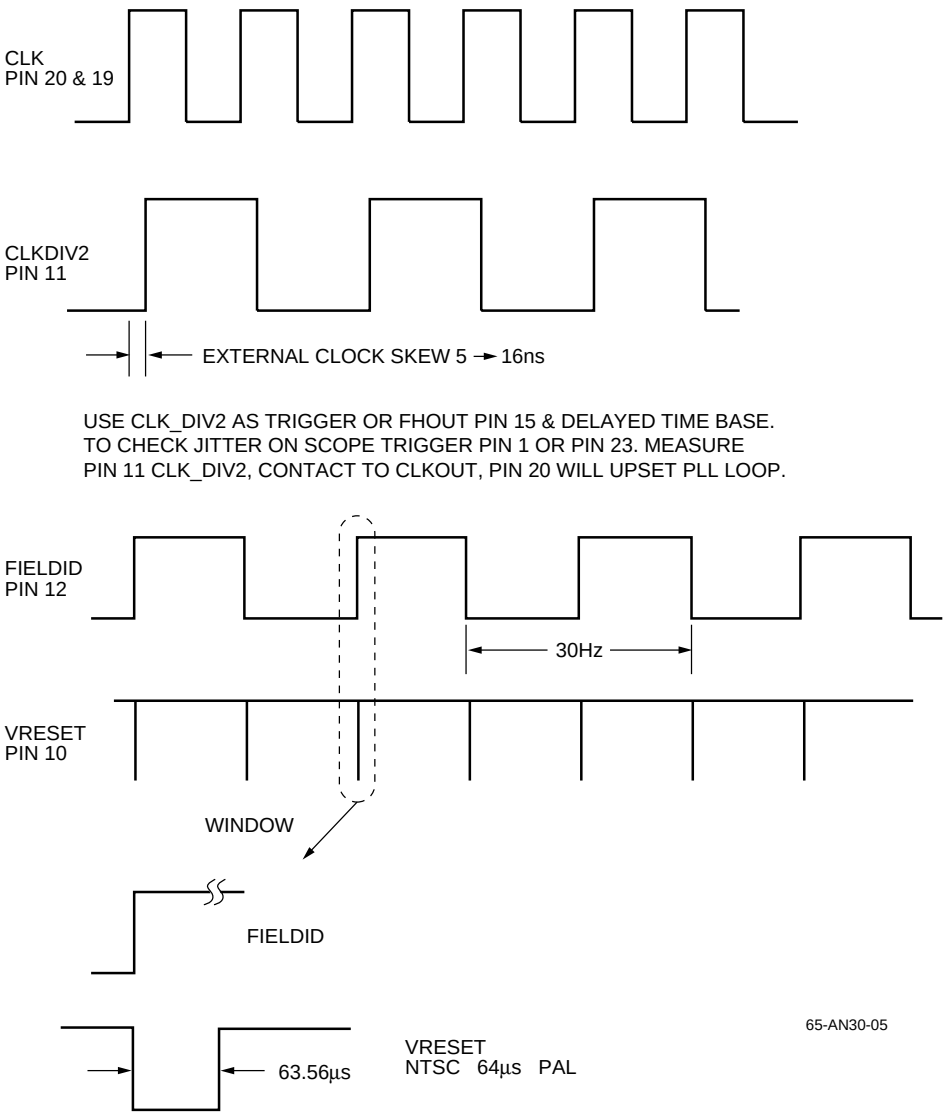


Figure 4. Device and Demo Board Waveform (continued)

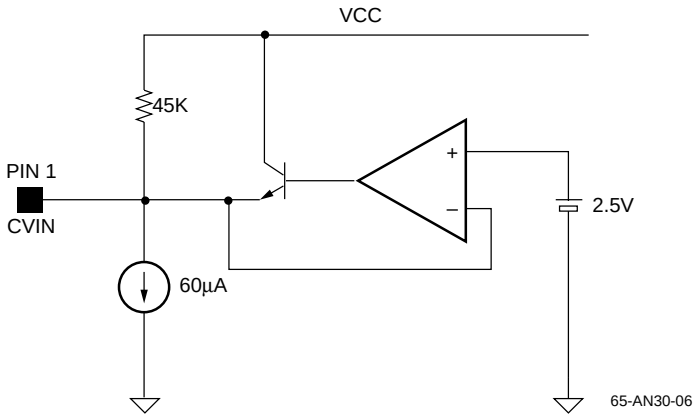


Figure 5. Input Structure for Sync Separator

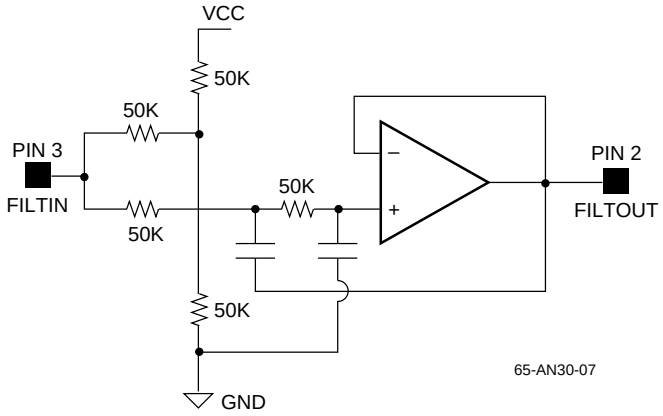


Figure 6. Input Filter Setup

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